

U.S. Patent Application No. 10/722,593

RECEIVED
CENTRAL FAX CENTER

Docket No. 4590-242

NOV 06 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended). A device to synthesize a range of frequencies F1-F2 with high spectral purity, comprising:

a variable-step synthesizer Na providing a range of frequencies F3-F4;

a variable ratio divider Nb connected to said variable step-synthesizer for receiving the range of frequencies from said variable-step synthesizer; and

a frequency control device adapted for delivering a division rank command of ~~[[the]]~~ a variable ratio divider, a command of the frequency of ~~[[the]]~~ said variable-step synthesizer, and a command of a synthesis step of ~~[[the]]~~ said variable-step synthesizer and connected at one output to said variable-step frequency synthesizer and at another output to said variable ratio divider,

wherein a length of the cycle of evolution of Na is variable and dependent on the value of Nb, ~~[[the]]~~ variable-step synthesizer is a fractional step phase-locked loop synthesizer.

2. (previously presented) The device according to claim 1 comprising a filtering device positioned after the variable ratio divider Nb.

3. (cancelled).

4. (previously presented) The device according to claim 1 wherein the variable ratio divider Nb is a value from N1 to Np, the values N1 to Np follow an arithmetic progression, and wherein a maximum frequency of the synthesizer is given by $F4=N1 \cdot F2$ where N1 is the smallest value of the sequence of values N1 to Np and the frequency F3 is a function of N2.

5. (previously presented) The device according to claim 4 wherein the value of the frequency F3 is substantially equal to or slightly lower than $(N1/N2) \cdot F4$.

U.S. Patent Application No. 10/722,593

Docket No. 4590-242

6. (previously presented) The device according to claim 1 wherein the variable ratio divider N_b is a value from N_1 to N_p , the values N_1 to N_p following a non-arithmetic progression.

7. (previously presented) The device according to claim 6 wherein F_3 is substantially equal to or smaller than a F_4 where a is the smallest value obtained in dividing two consecutive values one after the other.

8. (previously presented) The device according to claim 6 wherein the highest division rank N_b is chosen.

9. (previously presented) The device according to claim 1 further comprising a mixer receiving an output signal from the variable step synthesizer and a mixing signal.

10. (currently amended). A method of synthesizing a range of frequencies F_1 - F_2 with high spectral purity a frequency source which comprises the steps of:

dividing ~~[[the]]~~ an output signal of a voltage controlled oscillator by a first value N_b , and;
dividing an input signal of the voltage controlled by a second value N_a ,

wherein a length of ~~[[the]]~~ a cycle of evolution of N_a is variable and dependent on a value of N_b .

11. (previously presented) The method according to claim 10 wherein a value of N_b varies according to an arithmetic sequence $N_1 \dots N_p$ and wherein a frequency F_4 is determined by $N_1 * F_2$ and a frequency F_3 is a function of N_2 .

12. (previously presented) The method according to claim 11 wherein a value of the frequency F_3 is chosen to be substantially equal to or slightly below $(N_1/N_2) * F_4$.

13. (previously presented) The method according to claim 10 wherein a value of N_b varies according to a non-arithmetic sequence and wherein two consecutive values of the sequence are divided.

U.S. Patent Application No. 10/722,593

Docket No. 4590-242

14. (previously presented). The method according to claim 13 wherein F_3 is substantially equal to or smaller than a F_4 where a is the smallest value obtained in dividing two consecutive values of the sequence.

15. (previously presented). The method according to claim 14 wherein the highest division rank N_b is chosen.

16. (previously presented). The method according to claim 10, wherein the modification of the division rank and the synthesis step is simultaneous.

17. (previously presented). The method according to claim 1, wherein a ratio of a reference frequency to the frequency step, is a least common multiple of the sequence $N_1 \dots N_p$.

18. (original) The device according to claim 1 wherein reference frequency F_{ref} is chosen so that the desired fractional step values are obtained.

19. (original) The method according to claim 10 wherein the reference frequency F_{ref} is chosen so that the desired fractional step values are obtained as F_{ref} is a function of sequence of the values N_1, N_2, \dots, N_p assumed by N_b .

20. (original) The method according to claim 10 wherein the reference frequency F_{ref} is chosen so that the desired fractional step values are obtained as follows $F_{ref}/\Delta F$ must be a multiple of the LCM of N_1, N_2, \dots, N_p with ΔF a given frequency step.